CLAIMS:

1. A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating each of the plurality of binary outputs as a symmetric function of the binary inputs;

wherein said logic circuit is divided into a plurality of logic units, each logic unit is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to the logic unit, the binary inputs of said plurality of inputs are divided into inputs into a plurality of said logic units, and the binary outputs of said plurality of outputs are generated using binary outputs of a plurality of said logic units.

2. A parallel counter according to claim 1, wherein the binary inputs of said plurality of inputs are divided according to a binary tree into inputs into a plurality of said logic units.

3. A parallel counter according to claim 1, wherein said logic units are arranged to receive 2^n of said binary inputs, where n is an integer indicating the level of the logic units in the binary tree, said logic circuit has m logic units at each level, where m is a rounded up integer determined from (the number of binary inputs)/ 2^n, logic units having a higher level in the binary tree comprise logic of logic units at lower levels in the binary tree, and each logic unit is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to the logic unit.

4. A parallel counter according to claim 3, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as an elementary symmetric function of the binary inputs to said logic circuit.

5. A parallel counter according to claim 4, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to said logic circuit using OR logic for combining the binary inputs.

6. A parallel counter according to claim 5 wherein each logic unit at the first level is arranged to logically AND each of the binary inputs to the logic unit and to logically OR each of the binary inputs to the logic unit to generate the logic unit binary outputs.

7. A parallel counter according to claim 4, wherein each logic unit at the first level is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to said logic circuit using exclusive OR logic for combining the binary inputs.

8. A parallel counter according to claim 7 wherein each logic unit at the first level is arranged to logically AND each of the binary inputs to the logic unit and to logically exclusively OR each of the binary inputs to the logic unit to generate the logic unit binary outputs.

9. A parallel counter according to claim 3 wherein elementary logic units are provided as the logic units at the first level for performing elementary symmetric functions, outputs from each of two primary elementary logic units receiving four logically adjacent binary inputs from said plurality of inputs are input to two secondary elementary logic units, an output from each of the secondary elementary logic units is input to a tertiary elementary logic unit, and said primary, secondary and tertiary elementary logic units form a secondary logic unit at a second level of the binary tree having a binary output comprising a binary output from each of said secondary elementary logic units and two binary outputs from said tertiary elementary logic unit.

10. A parallel counter according to claim 9, wherein tertiary logic units at a third level of the binary tree each comprise two secondary logic units receiving eight logically adjacent binary inputs from said plurality of inputs, four elementary logic units receiving as inputs the outputs of said two secondary logic units, and further logic for generating

binary outputs as a symmetric function of the binary inputs to said tertiary logic unit using the binary outputs of said four elementary logic units.

11. A parallel counter according to claim 10, wherein quaternary logic units at a fourth level of the binary tree each comprise two tertiary logic units receiving sixteen logically adjacent binary inputs from said plurality of inputs, four elementary logic units receiving as inputs the outputs of said two tertiary logic units, and further logic for generating binary outputs as a symmetric function of the binary inputs to said quaternary logic unit using the binary outputs of said four elementary logic units

12. A parallel counter according to claim 3, wherein elementary logic units are provided as the logic units at the first level for performing elementary symmetric functions, and logic units for higher levels are comprised of logic units of lower levels.

13. A parallel counter according to claim 12, wherein said logic units for higher levels above the second level comprise logic units of an immediately preceding level and elementary logic units.

14. A parallel counter according to claim 3, wherein each logic unit at each level is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to said logic circuit using OR logic for combining the binary inputs.

15. A parallel counter according to claim 3, wherein each logic unit at each level is arranged to generate logic unit binary outputs as a symmetric function of the binary inputs to said logic circuit using exclusive OR logic for combining the binary inputs.

16. A logic circuit for multiplying two binary numbers comprising:
array generation logic for generating an array of binary numbers comprising all possible combinations of each bit of each binary number;
array reduction logic including at least one parallel counter according to any preceding claim for reducing the number of combinations in the array; and

binary addition logic for adding the reduced combinations to generate an output.

17. A method of designing a logic circuit comprising:

providing a library of logic module designs each for performing a small symmetric function;

designing a logic circuit to perform a large symmetric function;

identifying small symmetric functions which can perform said symmetric function;

selecting logic modules from said library to perform said small symmetric functions;

identifying a logic circuit in the selected logic circuit which performs a symmetric function and which can be used to perform another symmetric function;

selecting the logic circuit corresponding to the identified symmetric function and using the selected logic circuit with inverters to perform said other symmetric function using the relationship between the symmetric functions:

$$OR\_n\_k(X_1...X_n) = \neg OR\_n\_(n+1-k)(\neg X_1...\neg X_n)$$

where $\neg$ denotes an inversion, n is the number of inputs, and k is the number of sets of inputs AND combined together.

18. A conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter comprising the parallel counter according to ~~any one of claims 1 to 15~~ for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater than 2^p.

19. A constant multiplier comprising a conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter comprising the parallel counter according to ~~any one of claims 1 to 15~~ for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater than 2^p.

20. A digital filter comprising a conditional parallel counter having m possible high inputs out of n inputs, where m<n, and n and m are integers, the counter comprising the

parallel counter according to ~~any one of claims 1 to 15~~ Claim 1 for counting inputs to generate p outputs for m inputs, wherein the number n of inputs to the counter is greater than 2^p.

21. A parallel counter comprising:

a plurality of inputs for receiving a binary number as a plurality of binary inputs;

a plurality of outputs for outputting binary code indicating the number of binary ones in the plurality of binary inputs; and

a logic circuit connected between the plurality of inputs and the plurality of outputs and for generating each of the plurality of binary outputs as a symmetric function of the binary inputs.

22. A parallel counter according to claim 21 wherein said logic circuit is arranged to generate at least one of the binary outputs as a symmetric function of the binary inputs using exclusive OR logic for combining a plurality of sets of one or more binary inputs.

23. A parallel counter according to claim 22 wherein said logic circuit is arranged to logically AND members of each set of binary inputs and to logically exclusively OR the result of the AND operations.

24. A parallel counter according to claim 23 wherein said logic circuit is arranged to logically AND 2^i of the binary inputs in each set for the generation of the i^{th} binary output, where i is an integer from 1 to N, N is the number of binary outputs and i represents the significance of each binary output, each set being unique and the sets covering all possible combinations of binary inputs.

25. A parallel counter according to claim 23 wherein said logic circuit is arranged to logically AND members of each set of binary inputs, where each set is unique and the sets cover all possible combinations of binary inputs.

26. A parallel counter according to claim 21 wherein said logic circuit is arranged to generate at least one of the binary outputs as a symmetric function of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs.

27. A parallel counter according to claim 26 wherein said logic circuit is arranged to logically AND members of each set of binary inputs and to logically OR the result of the AND operations.

28. A parallel counter according to claim 27 wherein said logic circuit is arranged to logically AND 2^{N-1} of the binary inputs in each set for the generation of the N^{th} binary output, where N is the number of binary outputs and the N^{th} binary output is the most significant, each set being unique and the sets covering all possible combinations of binary inputs.

29. A parallel counter according to claim 27 wherein said logic circuit is arranged to logically AND members of each set of binary inputs, where each set is unique and the sets cover all possible combinations of binary inputs.

30. A parallel counter according to claim 21 wherein said logic circuit is arranged to generate a first binary output as a symmetric function of the binary inputs using exclusive OR logic for combining a plurality of sets of one or more binary inputs, and to generate an N^{th} binary output as a symmetric function of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs.

31. A parallel counter according to claim 21 wherein said logic circuit is arranged to generate two possible binary outputs for a binary output less significant than the N^{th} binary output, as symmetric functions of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs where N is the number of binary outputs, the sets used for each possible binary output being of two different sizes which are a function of the binary output being generated; and said logic circuit including selector

logic to select one of the possible binary outputs based on a more significant binary output value.

32. A parallel counter according to claim 31 wherein said logic circuit is arranged to generate the two possible binary outputs for the $(N-1)^{th}$ binary output less significant than the N^{th} binary output, as symmetric functions of the binary inputs using OR logic for combining a plurality of sets of one or more binary inputs, the sets used for each possible binary output being of size $2^{N-1} + 2^{N-2}$ and 2^{N-2} respectively and said selector logic being arranged to select one of the possible binary outputs based on the N^{th} binary output value.

33. A parallel counter according to claim 21 wherein said logic circuit includes a plurality of subcircuit logic modules each generating intermediate binary outputs as a symmetric function of some of the binary inputs, and logic for logically combining the intermediate binary outputs to generate said binary outputs.

34. A parallel counter according to claim 33 wherein said subcircuit logic modules are arranged to use OR logic for combining sets of said some of said binary inputs.

35. A parallel counter according to claim 34 wherein said logic circuit includes one or more logic modules each for generating a binary output as a symmetric function of the binary inputs using executive OR logic for combining a plurality of sets of one or more binary inputs.

36 A logic circuit for multiplying two N bit binary numbers, the logic circuit comprising:

array generation logic for performing the logical AND operation between each bit in one binary number and each bit in the other binary number to generate an array of logical AND combination comprising an array of binary values, and for further logically combining values to generate the array in which the maximal depth of the array is below N bits;

array reduction logic for reducing the depth of the array to two binary numbers; and

addition logic for adding the binary values of the two binary numbers.

37. A logic circuit according to claim 36 wherein said array generation logic is arranged to perform the further logical combination of values for values formed by the logical AND combination of each bit A_i of one binary number and each bit B_j of the other binary number, where $i-j-k \leq 1$, k is a chosen integer, and i and j are integers from 1 to N.

38. A logic circuit according to claim 36 wherein said array generation logic is arranged to logically AND combine each bit A_i of the first binary number with each bit B_j of a second binary number to generate said array comprising a sequence of binary numbers represented by said logical AND combinations, A_i AND B_j and to carry out further logical combination by logically combining the combination A_1 AND B_{N-2}, A_1 AND B_{N-1} where N is the number of bits in the binary numbers.

39. A logic circuit according to claim 38 wherein said array generation logic is arranged to combine the combinations A_1 AND B_{N-2} and A_0 AND B_{N-1}, using exclusive OR logic to replace these combinations, and to combine A_1 AND B_{N-1} and A_0 AND B_{N-2} to replace the A_1 AND B_{N-1} combination.

40. A logic circuit according to claim 36 wherein said array reduction logic includes at least one of: at least one full adder, at least one half adder, and at least one parallel counter.

41. A logic circuit according to claim 40 wherein said array reduction logic includes at least one parallel counter according to ~~any one of claims 1 to 16 or 21 to 35.~~